

EVAL-AD766XCB/AD767XCB

OPERATING THE EVAL-AD766XCB/AD767XCB

The EVAL-AD766XCB/AD767XCB is a four-layer board carefully laid out and tested to demonstrate the specific high accuracy performance of the AD766X/AD767X. Figure 1 shows the schematics of the evaluation board. The layouts of the board are given in :

Top side silk-screen - Figure 2

Top side layer - Figure 3

Ground layer - Figure 4

Shield layer - Figure 5

Bottom side layer - Figure 6

Bottom side silk-screen - Figure 7.

The EVAL-AD766XCB/AD767XCB is a flexible design that enables the user to choose among many different board configurations. A description of each selectable jumper/switch is listed in Table II and the available test points are listed in Table III. Note that the button of a switch in position A (U3 side) defines a low level.

The EVAL-AD766XCB/AD767XCB is configured in factory with 0 to 2.5 V ADC input range for the AD7660, AD7664, and AD7675/7676/7677 and +/-5V for the AD7663/7665/7671; front-end amplifiers U6 and U7 set with a gain of +1, powered through the EVAL-CONTROL BOARD, and the on-board $\overline{\text{CNVST}}$ generation used.

On-board or external $\overline{\text{CNVST}}$ could be used. When an external $\overline{\text{CNVST}}$ signal is applied, this signal should have very low jitter and sharp edges to get the best noise performance of the part. Meanwhile, it is recommended to use the on-board $\overline{\text{CNVST}}$ generation which is done by dividing MCLK signal (20MHZ) by the numbers shown in Table I, which are entered in the software. Activity on BUSY pin of the ADC turns on the LED.

Table I. $\overline{\text{CNVST}}$ GENERATION

| Part | Division Factor | Throughput Rate |
|-----------|-----------------|-----------------|
| AD7660 | 200 | 100KSPS |
| AD7662/68 | 40 | 500KSPS |
| AD7663 | 80 | 250KSPS |
| AD7664/50 | 35 | 571KSPS |
| AD7665 | 35 | 571KSPS |
| AD7671 | 20 | 1MSPS |
| AD7675 | 200 | 100KSPS |
| AD7676 | 35 | 571KSPS |
| AD7677 | 20 | 1MSPS |

Conversion data is available at the output bus BD on U3, on the 40-pin connector P2, and on the 96-pin connector P3. Additionally, BD data is updated on the falling/rising edge of $\overline{\text{DBUSY}}$ and $\overline{\text{BBUSY}}$ on P3, low when BD data is valid are delayed from the BD data by about 20 ns to ease the interface. When either parallel or serial reading mode of the ADC is used, the data is available on this parallel bus. When serial reading mode of the ADC is used, the serial interface signals of the ADC are buffered and available on the 20-pin connec-

tor P1. When slave serial reading mode of the AD766X/AD767X is used, the external serial clock SCLK applied to the ADC is at half the MCLK frequency.

Power Supplies and Grounding

The evaluation board ground plane is separated into two sections: a plane for the digital interface circuitry and an analog plane for the analog input and external reference circuitry. To attain high resolution performance, the board was designed to ensure that all digital ground return paths do not cross the analog ground return paths.

The EVAL-AD766XCB/AD767XCB has three power supply blocks: a single 5V supply VA (SJ1) for the AD766X/AD767X and the reference voltage circuitry, a digital 5V supply VL (SJ2) for the digital interface circuitry and the digital section of the ADC, and a selectable +/-12V (with a possibility of +/-15V with control Brd2) or +/-5V supply for the analog signal conditioning circuitry (SJ3). All supplies are decoupled to ground with 10 μF tantalum and 0.1 μF ceramic capacitors.

Analog Input Ranges

The analog front-end amplifier circuitry U6 and U7 allows flexible configuration changes such as positive or negative gain, input range scaling, filtering, addition of a DC component, use of different op-amp and supplies.

Figure 1 shows the front end op-amp configuration used with the AD7660/7663/7664/7665/7671/7675/7676/7677.

In some applications, it is desired to use a bipolar or wider analog input range like, for instance, $\pm 10\text{V}$, $\pm 5\text{V}$, $\pm 2.5\text{V}$, or 0 to +5V. For the AD76XX parts which do not have directly those input ranges like the AD7660/7664/7675/7676/7677, by simple modifications of the input driver circuitry of the EVAL-AD766XCB/AD767XCB, bipolar and wider input ranges can be used without any performance degradation. Components values required and resulting full-scale ranges are shown in table IV and table V.

In factory, the analog input of U6 is set at mid-scale ($R6=R7=590\Omega$) for the AD7660/7664/7675/7676/7677. For AD7663/7665/7671, R7 is not connected to maintain the input at 0V (mid-scale). This allows a transition noise test without any other equipment. An FFT test can be done by applying a very low distortion AC source.

EVAL-CONTROL BOARD INTERFACE

The EVAL-AD766XCB/AD767XCB interfaces to the EVAL-CONTROL BRD2 through the 96-way connector.

RUNNING THE EVAL-AD766X/AD767XCB SOFTWARE

Software Description

The EVAL-AD766XCB/AD767XCB comes with software for analyzing the AD766X/AD767X. Through the EVAL-CONTROL BRD2 one can perform a histogram to determine code transition noise, and Fast Fourier Transforms (FFT's) to determine the Signal-to-Noise Ratio (SNR), Signal-to-Noise-plus-Distortion (SNRD) and Total-Harmonic-Distortion (THD). The front-end PC software has four screens as shown in Figure 8,9,10 and 11. Figure 8 is the Setup Screen where input voltage range, sample rate, number of samples are selected. Figure 9 is the Histogram Screen, which allows the code distribution for DC input and computes the mean

Figure 10 is the FFT Screen, which performs an FFT on the captured data, computes the Signal-to-Noise Ratio (SNR), Signal-to-Noise-plus-Distortion (SINAD) and total-Harmonic-Distortion (THD). Figure 11 is the time domain representation of the output. When the on-board $\overline{\text{CNVST}}$ generation is used, a synchronous FFT could be achieved by synchronizing the external AC generator with the Fsync signal (TP11) which is an exact division by 2 of MCLK.

Software Installation

- Double-Click on Setup.exe from the CD-ROM and follow the installation instructions.

NOTE: The software runs under Windows 95/98 only.

TABLE II. JUMPER DESCRIPTION

| Jumper Designation | Default position with the control board (Factory settings) | Function |
|--------------------|---|--|
| JP1 | A | Selection of the positive supply of the front-end amplifier U6. When JP1 is in position A, the +12V supply from the control board is applied to JP3 otherwise VS+ on SJ3 is used. |
| JP2 | A | Selection of the negative supply of the front-end amplifier U6. When JP2 is in position A, the -12V supply from the control board is applied to JP4 otherwise VS- on SJ3 is used. |
| JP3 | A | Selection of the positive supply of the front-end amplifier U6. When JP3 is in position A, the +5V supply from the control board is used otherwise JP1 output is used. |
| JP4 | A | Selection of the negative supply of the front-end amplifier U6. When JP4 is in position A, the -5V supply from the control board is used otherwise JP2 output is used. |
| JP5 | not A | Selection of the master clock MCLK signal. When JP5 is in position A, the signal on J4 is used otherwise the on-board 20 MHz $\overline{\text{CNVST}}$ clock is used as a MCLK signal. MCLK signal is used to generate the on-board $\overline{\text{CNVST}}$ signal and the external serial clock SCLK. |
| JP6 | A, U3 side | Selection of RDC (Read during convert). When the button of the switch is close to J4 connector (not A position) and when the serial reading mode is selected, the data are read during conversion otherwise the data are read after conversion. JP6 has no use in parallel reading mode. |
| JP7 | A, U3 side | Selection of PD (Powerdown). When the button of the switch is close to J4 connector (not A position), the ADC is in power-down mode. |
| JP8 | A, U3 side | Spare switch. |
| JP9 | A, U3 side | Selection of RESET. When the button of the switch is close to J4 connector (not A position), the ADC is reset. |
| JP10 | A, U3 side | Selection of $\overline{\text{SER/PAR}}$ (serial/parallel reading mode). When the button of the switch is close to J4 connector (not A position), the data are read in serial mode otherwise the data are read in parallel mode. |
| JP11 | not A, SJ4 side | Selection of $\overline{\text{OC/2C}}$ (coding). When the button of the switch is close to J4 connector (not A position), the ADC uses a straight binary coding otherwise the twos complement coding is used. |
| JP12 | A, U3 side | Selection of WARP. When the button of the switch is close to J4 connector (not A position), the ADC uses the WARP mode which is the fastest one. With the AD7660, JP12 is a spare switch. |

EVAL-AD766XCB/AD767XCB

TABLE II. JUMPER DESCRIPTION

| Jumper Designation | Default position with the control board (Factory settings) | Function |
|---------------------------|--|--|
| JP13 | A, U3 side | Selection of IMPULSE. When the button of the switch is close to J4 connector (not A position), the ADC uses the IMPULSE mode which is the mode with the lowest power dissipation. With the AD7660, JP13 is a spare switch. |
| JP14 | A, U3 side | TEST1. For factory use only and it is pull down. |
| JP15 | A, U3 side | TEST0. For factory use only and it is pull down. |
| JP16 | A, U3 side | Selection of $\overline{\text{EXT/INT}}$ (use of external or internal serial clock). When the button of the switch is close to J4 connector (not A position) and when the serial reading mode is selected, the data are read with an external serial clock SCLK generated from the master clock MCLK otherwise the data are read with the ADC serial clock. When external serial clock reading mode is selected, MCLK has to be fast enough to be able the read the data properly as explained in the AD766X data sheet. JP16 has no use in parallel reading mode. |
| JP17 | A, U3 side | Selection of $\overline{\text{INVS}}\overline{\text{SYNC}}$ (SYNC active level). When the button of the switch is close to J4 connector (not A position) and when the master serial reading mode is selected, the SYNC signal is active Low. JP17 has no use in parallel reading mode or slave serial reading mode. |
| JP18 | A, U3 side | Selection of $\overline{\text{INVS}}\overline{\text{CLK}}$ (SCLK active edge). When the button of the switch is close to J4 connector (not A position) and when the serial reading mode is selected, $\overline{\text{INVS}}\overline{\text{CLK}}$ is high. JP18 has no use in parallel reading mode. |
| JP19 | not A | Selection of $\overline{\text{CNV}}\overline{\text{ST}}$ signal. When JP19 is in position A, the signal on J3 is used otherwise the on-board $\overline{\text{CNV}}\overline{\text{ST}}$ generation is used. MCLK signal is used to generate the on-board $\overline{\text{CNV}}\overline{\text{ST}}$ signal. |
| JP20 | not A | Selection of REF signal. When JP20 is in position A, the REF is buffered. When JP20 is not in position A, the REF is not buffered. |

Table III. EVAL-AD766XCB/AD767XCB Test Points

| Test Point | Available Signal |
|-------------------|--|
| TP1 | DGND Digital ground |
| TP2 | DGND Digital ground |
| TP3 | SIG+ ADC Analog input |
| TP4 | AGND Analog ground close to SIG+ |
| TP5 | REF ADC Reference input |
| TP6 | BUSY ADC BUSY signal |
| TP7 | $\overline{\text{RD}}$ ADC $\overline{\text{RD}}$ signal |
| TP8 | $\overline{\text{CS}}$ ADC $\overline{\text{CS}}$ signal |
| TP9 | AGND Analog ground close to REF |
| TP10 | $\overline{\text{CNV}}\overline{\text{ST}}$ ADC $\overline{\text{CNV}}\overline{\text{ST}}$ signal |
| TP11 | $\overline{\text{F}}\overline{\text{SYNC}}$ MCLK divided by 2 |
| TP12 | OVDD ADC digital output supply |
| TP13 | DVDD ADC digital core supply |
| TP14 | VANA1 ADC analog supply |
| TP15 | AGND Analog ground close to SIG- |
| TP16 | SIG- ADC Analog input |

Table IV. Component values Vs. Input ranges (AD7660)

| Input range | R1 | R3 | R6 | R7 |
|--------------------|-------------|-------------|----------------|--------------|
| $\pm 10\text{V}$ | 8k Ω | 1k Ω | 8k Ω | 10k Ω |
| $\pm 5\text{V}$ | 8k Ω | 2k Ω | 6.67k Ω | 10k Ω |
| 0 to -5V | 8k Ω | 8k Ω | 0 Ω | none |

Table V. Component values Vs. Input ranges (AD7664)

| Input range | R1 | R3 | R6 | R7 |
|--------------------|-------------|--------------|----------------|--------------|
| $\pm 10\text{V}$ | 2k Ω | 250 Ω | 8k Ω | 10k Ω |
| $\pm 5\text{V}$ | 2k Ω | 500 Ω | 6.67k Ω | 10k Ω |
| 0 to -5V | 1k Ω | 1k Ω | 0 Ω | none |

TESTING METHODS**Histogram**

To perform a histogram test, apply a DC signal to the input. It is advised to filter the signal to make the DC Source noise compatible with that of the ADC. C26 provides this filtering.

AC Testing

To perform an AC test, apply a sinusoidal signal to the evaluation board. Low distortion, better than 100dB, is required to allow true evaluation of the part. One possibility is to filter the input signal from the AC source. There is no suggested bandpass filter but consideration should be taken in the choice. Furthermore, when the full-scale input range is more than a few Vpp, it is recommended that you use the on board amplifier to amplify the signal, thus preventing the filter from distorting the input signal.

Please refer to Figures 8,9,10 and 11 to see the screens of the software.

Software Description

The AD16bit.exe is the software which allows you to analyze different performance characteristics of the AD766X, AD767X, AD97X and AD67X 16-bit ADC family. The software allows you to test the histogram as well as perform different AC tests.

Setup Requirements

- Evaluation Control Board 2 (ADSP2189)
- Evaluation Board
- Power Supply (AC 15V/1A source could be bought from ADI)
- Parallel Port Cable (provided with the evaluation control board)
- AC Source (low distortion)
- DC Source (low noise)
- Bandpass Filter (value based on your signal frequency, low distortion)

USE OF EVAL-AD766XCB/AD767XCB AS STAND-ALONE EVALUATION BOARD

You have the option of using the EVAL-AD766XCB/AD767XCB as a stand-alone evaluation board. This method does not require the control board, nor does it require use of the accompanied software. The digital output will now be available on P1 (20-pin connector, for use in serial mode) or P2 (40-pin connector, for use in parallel mode). Certain modifications have to be made on the board to allow proper operation of the evaluation board. Refer to Table II to obtain the jumper positions for stand-alone operation. When in stand-alone, $\overline{\text{CNVST}}$ could be externally applied or is generated internally according to Table I.

Please refer to Figure 1 to obtain the data output pins on the connectors.

Data is updated on the falling edge of BUSY. $\overline{\text{BCS}}$ and $\overline{\text{BWR}}$ are inputs to the FPGA and are connected to P1 and P2. When $\overline{\text{BCS}}$, CONTROL are low and $\overline{\text{BWR}}$ is high, which is the default value defined by the on-board pull-up/pull-down resistors, the data bus BD available on the P2 connector is enabled.

SUPPLYING THE BOARD FOR STAND-ALONE USE

SJ1 is the analog supply. Connect VA+ to +5V and AGND to GND. SJ2 is the digital supply. SJ2 requires the same values as SJ1, and SJ2 may be connected to SJ1. SJ3 is the supply for the front end amplifier (U6). Connect +12V to VS+, GND to AGND, and -12V to VS-.

EVAL-AD766XCB/AD767XCB**EVAL-BOARD SETTING FOR INPUT CONFIGURATIONS**

The AD7663/AD7665 and AD7671 have the ability to operate both unipolar and bipolar range. The available options are +/- 10V, +/- 5V, +/- 2.5V, 0 to 10V, 0 to 5V and 0 to 2.5V.

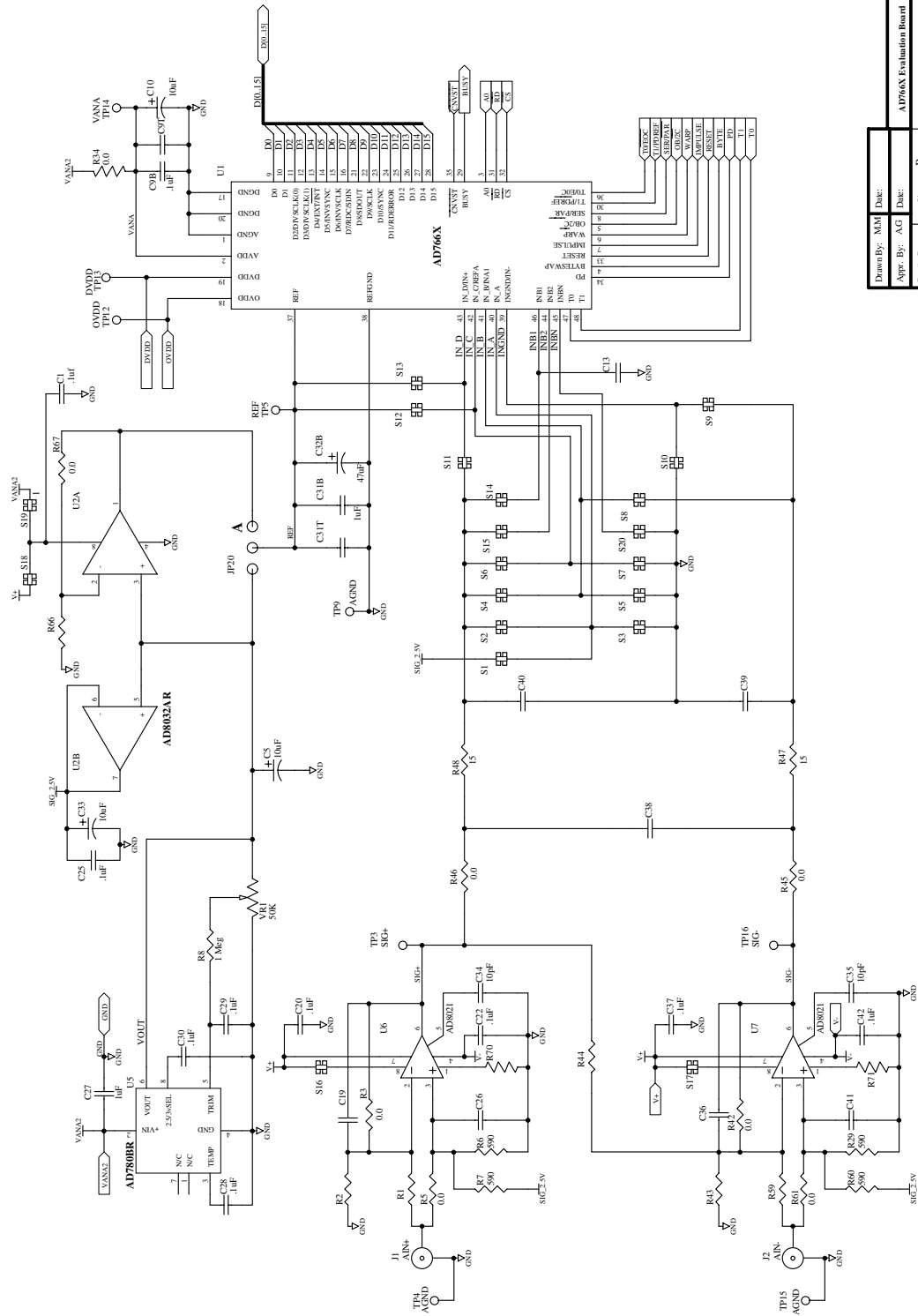
Table VI shows the required configurations for each input range. (REF = 2.5V). Table VII lists the default settings of the board for all parts.

Table VI. AD7663/7665/7671 Analog Input Configuration

| Input Voltage Range | IND(4R) | INC(4R) | INB(2R) | INA(R) |
|----------------------------|-----------------|-----------------|-----------------|-----------------|
| ±4 REF | V _{IN} | INGND | INGND | REF |
| ±2 REF | V _{IN} | V _{IN} | INGND | REF |
| ±REF | V _{IN} | V _{IN} | V _{IN} | REF |
| 0 V to 4REF | V _{IN} | V _{IN} | INGND | INGND |
| 0 V to 2REF | V _{IN} | V _{IN} | V _{IN} | INGND |
| 0 V to REF | V _{IN} | V _{IN} | V _{IN} | V _{IN} |

Table VII. Default Settings

| Component/Part | R7 | S9 | S10 | R48 | C40 | R47 | C39 |
|-----------------------|-----------|-----------|------------|------------|------------|------------|------------|
| AD7660 | 590Ω | None | 0Ω | 0Ω | None | | |
| AD7663 | None | None | 0Ω | 0Ω | None | | |
| AD7664 | 590Ω | None | 0Ω | 15Ω | 2.7nF | | |
| AD7665 | None | None | 0Ω | 0Ω | None | | |
| AD7671 | None | None | 0Ω | 0Ω | None | | |
| AD7675 | 590Ω | 0Ω | None | 15Ω | 2.7nF | 15Ω | 2.7nF |
| AD7676 | 590Ω | 0Ω | None | 15Ω | 2.7nF | 15Ω | 2.7nF |
| AD7677 | 590Ω | 0Ω | None | 15Ω | 2.7nF | 15Ω | 2.7nF |

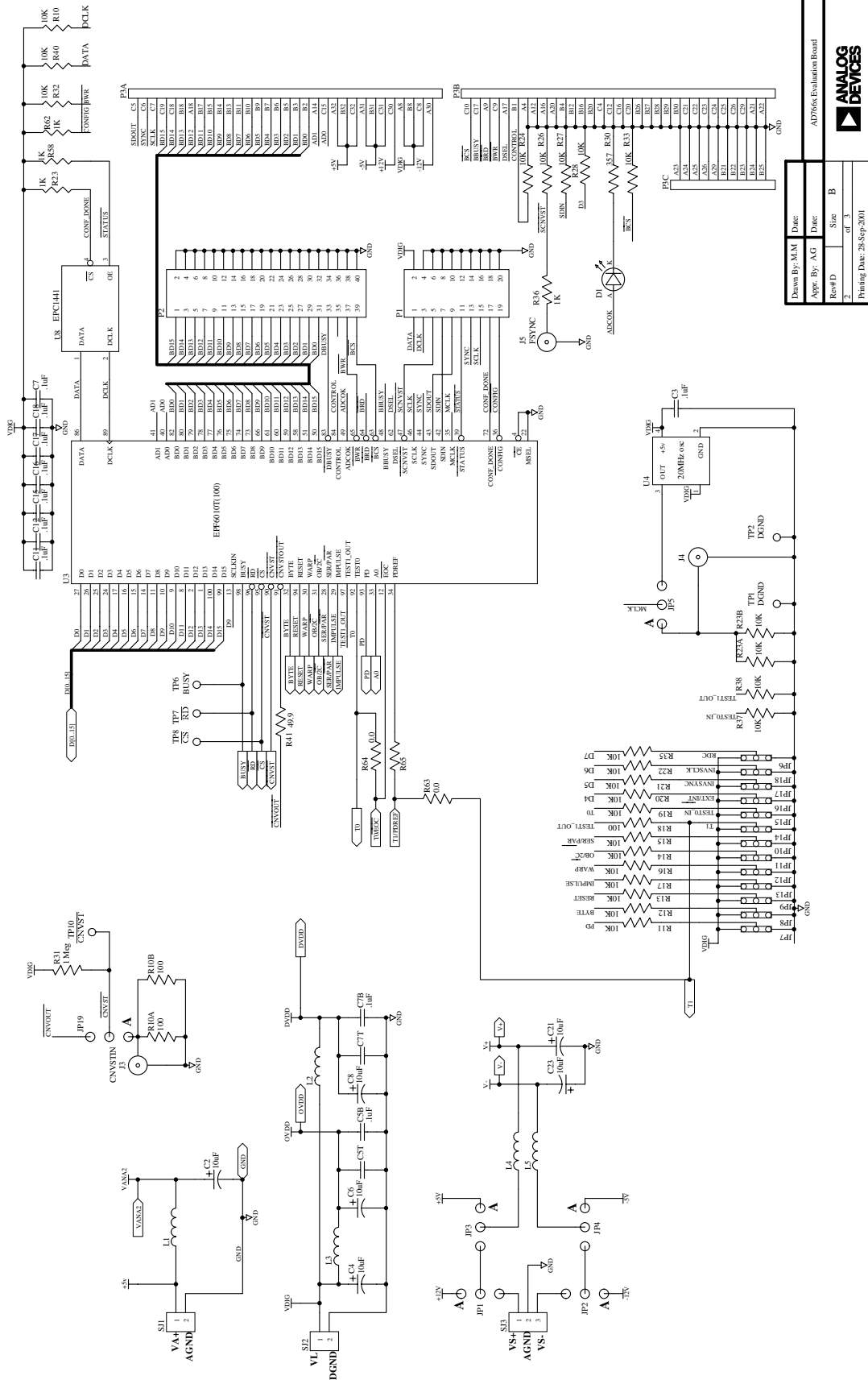


| | | | |
|---------------|-------|-------------------------|---------------------------|
| Drawn By: MAM | Date: | AD766X Evaluation Board | |
| Appr. By: AG | Date: | Rev# | Size |
| | | D | B |
| | | of | 3 |
| | | Sheet 2 | Printing Date: 4-Oct-2001 |



Figure 1. Schematic

EVAL-AD766XCB/AD767XCB



| | |
|----------------------------|--------|
| Drawn By: M.M | Date: |
| Appr. By: A.G | Date: |
| Rev# D | Size B |
| 2 | of 3 |
| Printing Date: 28-Sep-2001 | |



Figure 1 Schematic

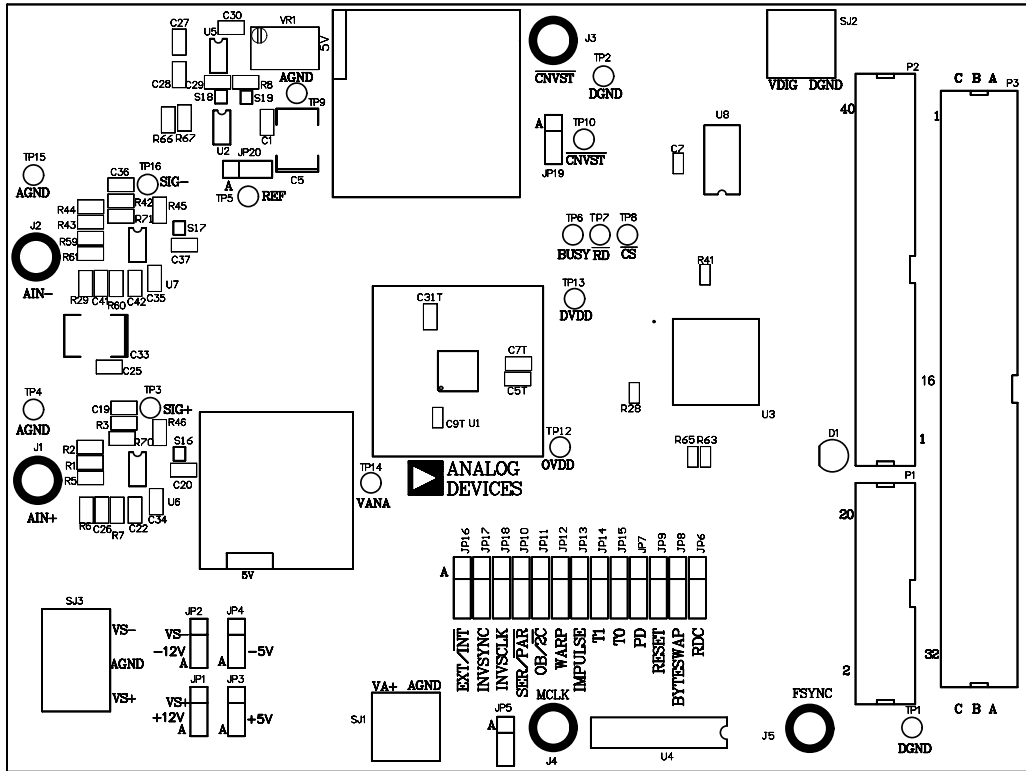


Figure 2. Top side silk-screen (Not to Scale).

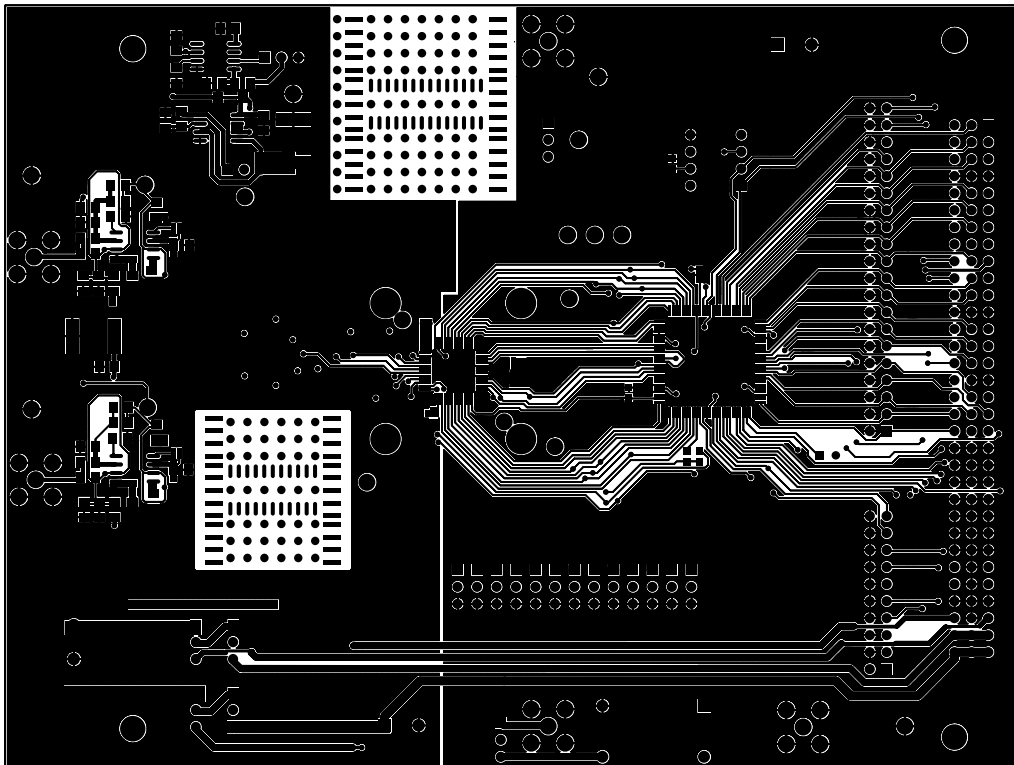


Figure 3. Top side (Not to Scale).

EVAL-AD766XCB/AD767XCB

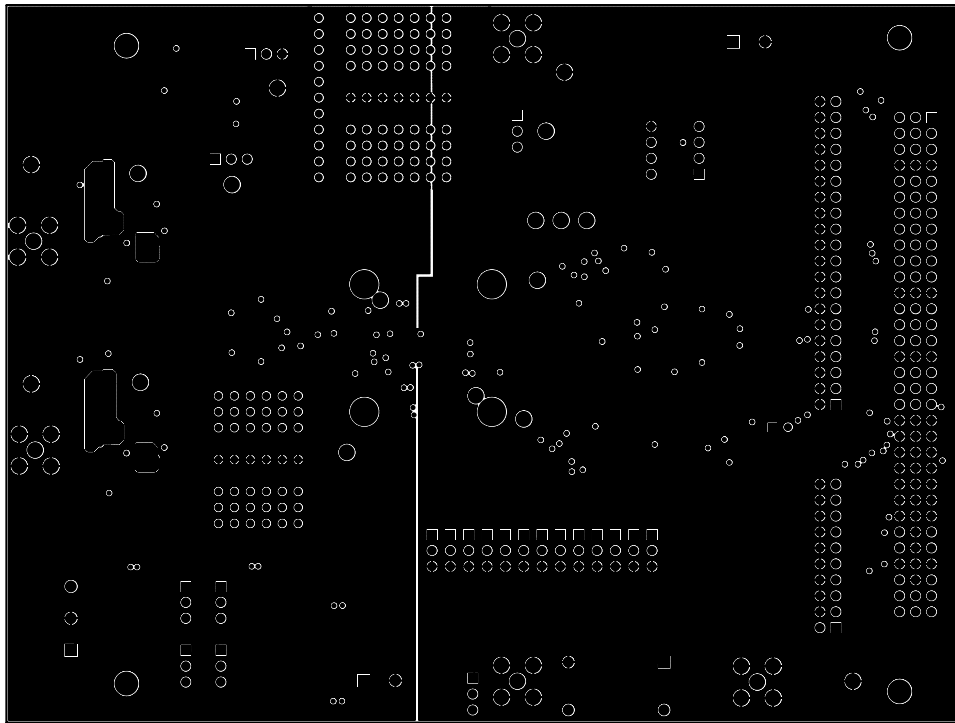


Figure 4. Ground Layer (Not to Scale).

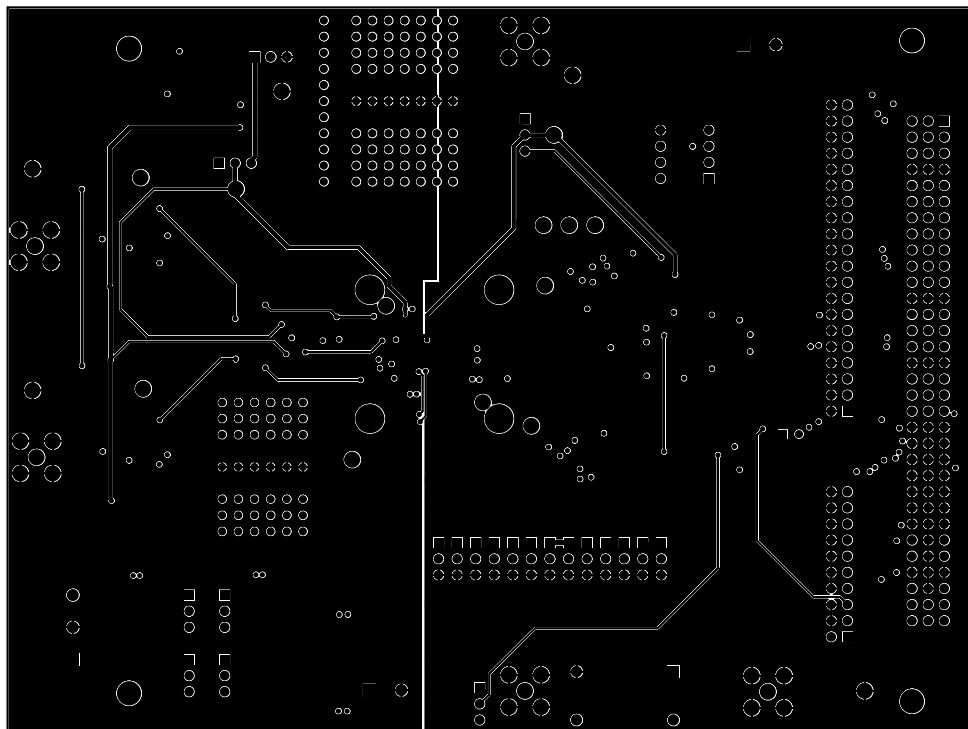


Figure 5. Shield Layer (Not to Scale).

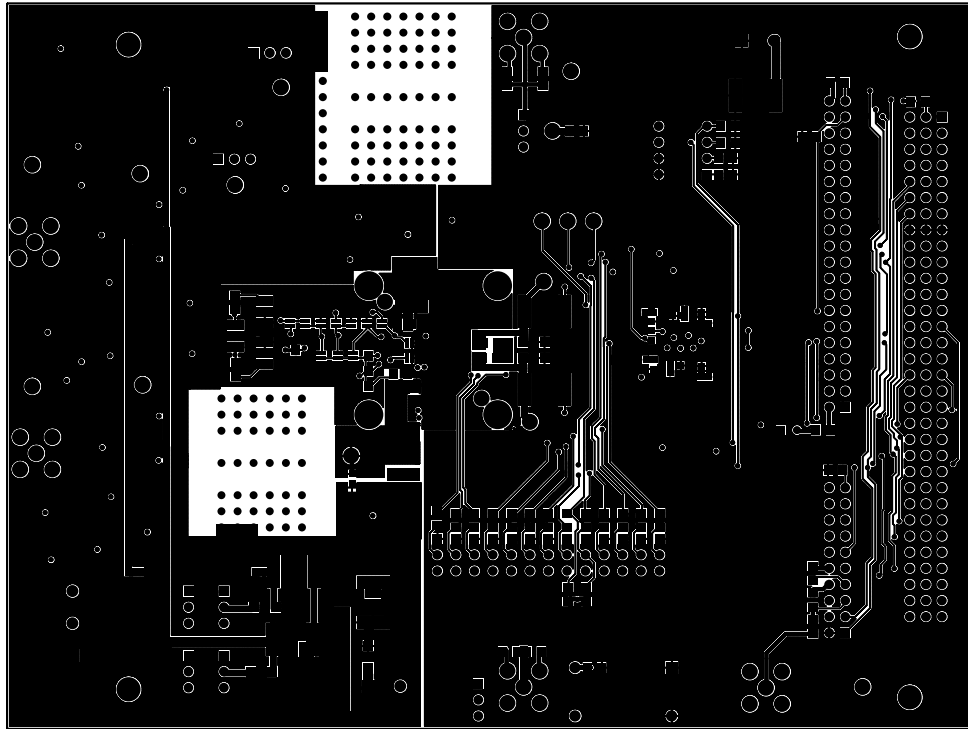


Figure 6. Bottom side layer (Not to Scale).

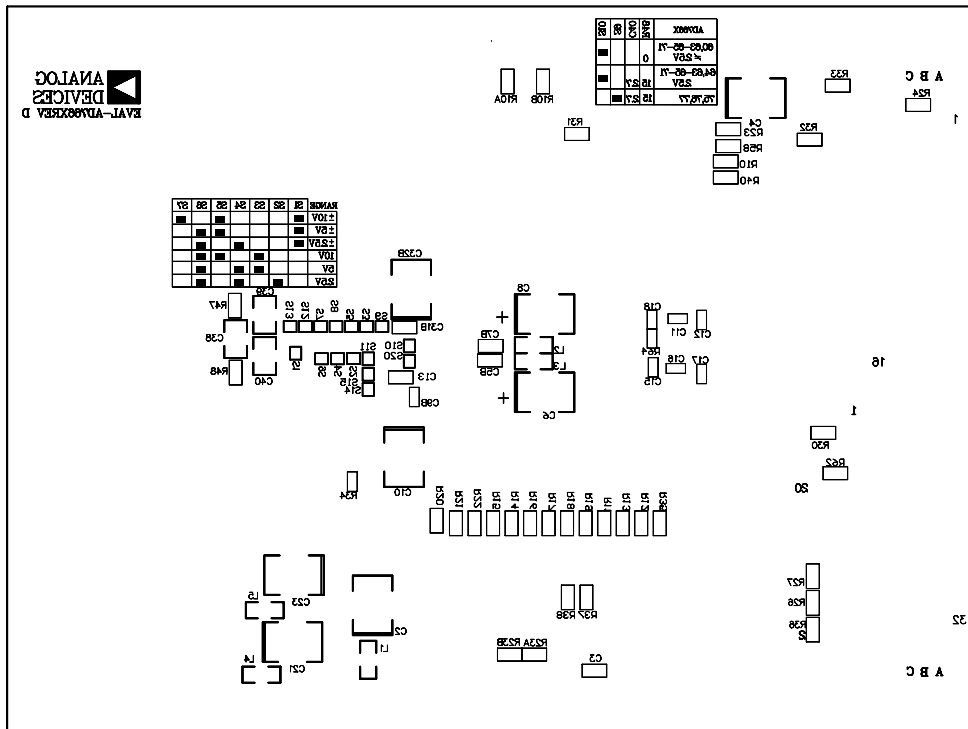


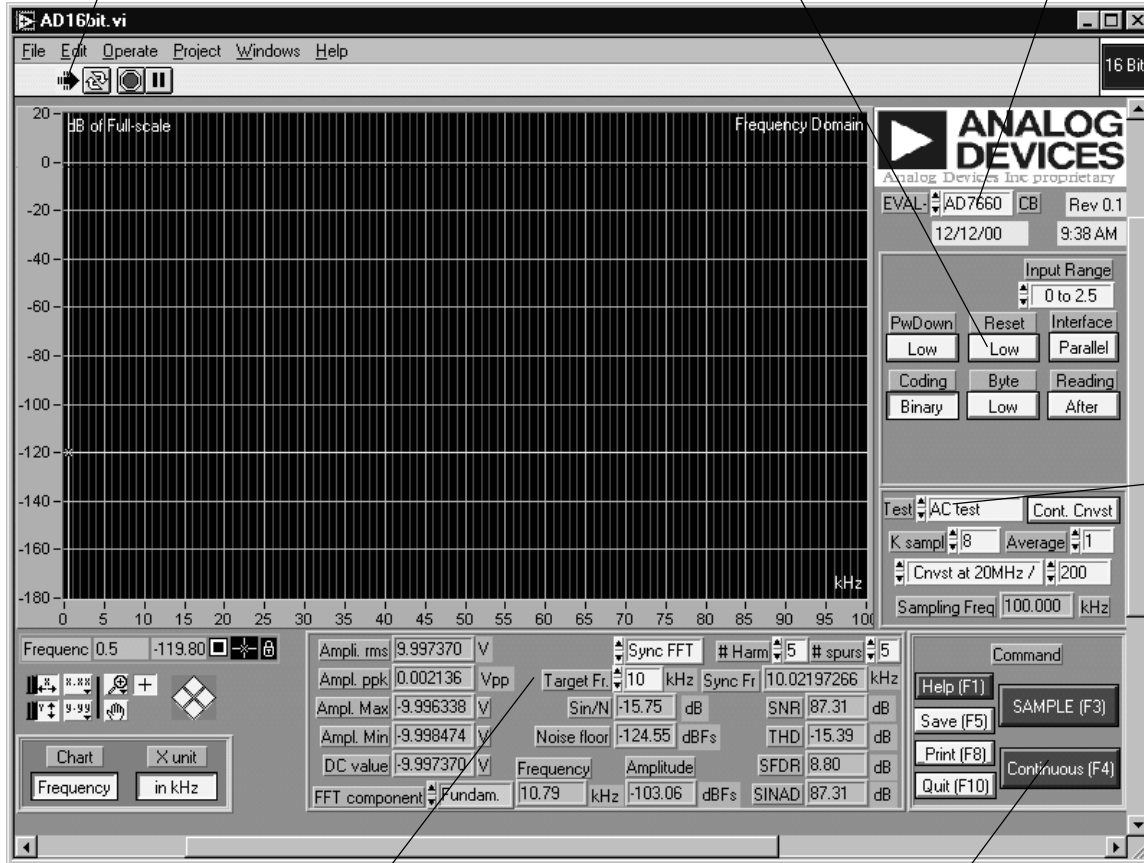
Figure 7. Bottom side silk-screen (Not to Scale).

EVAL-AD766XCB/AD767XCB

1) The Run button starts the software. All input configurations are read by the software after running the software. You will need to press this button first.

2) The part under evaluation is chosen from this menu. The available choices are AD766X, AD97x and AD67x.

3) Input Configurations are chosen here. For the AD766X/AD767X, the available choices are: PwDown, Reset, Interface, Coding, Byte, and Reading.



4) The choice of test is made here. You may choose to perform either a Histogram test or an AC test.

Figure 8. Setup Screen

This is the performance window.

5) You may choose to take one sample (Sample,F3), or perform continuous sampling (Continuous,F4). You may also choose the Help, Save, Print or Quit options. The Help menu will show you a description of the functionality of the chosen command.

The results are displayed on this chart. You may also use the cursor (yellow) and drag it to your desired location, where the X-axis value and the Y-axis value will be displayed.

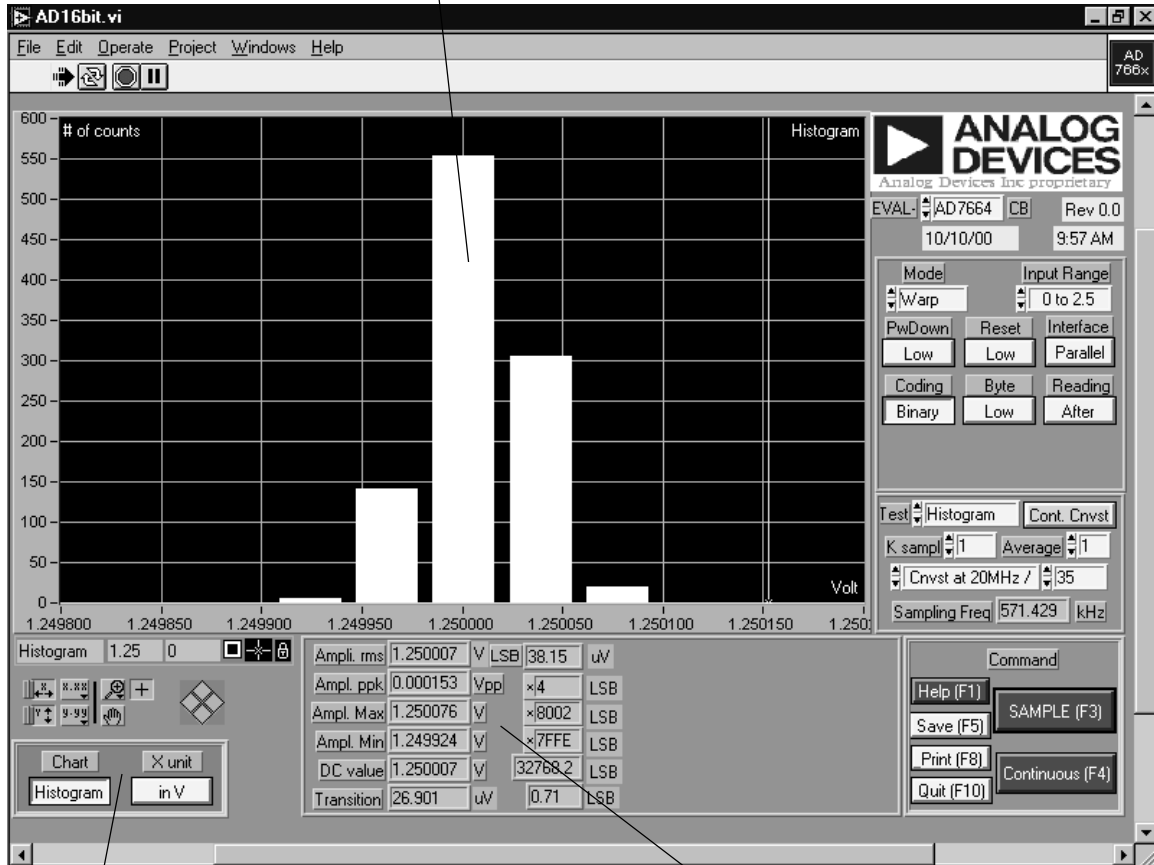


Figure 9. Histogram Screen

This control allows you the choice of display. You have the option of Time or Histogram. You also have the option of changing the X-axis unit

Different measurements are displayed here. The DC value, transition noise, and other values.

EVAL-AD766XCB/AD767XCB

The results are displayed on this chart. You may also use the cursor (yellow) and drag it to your desired location, where the X-axis value and the Y-axis value will be displayed.

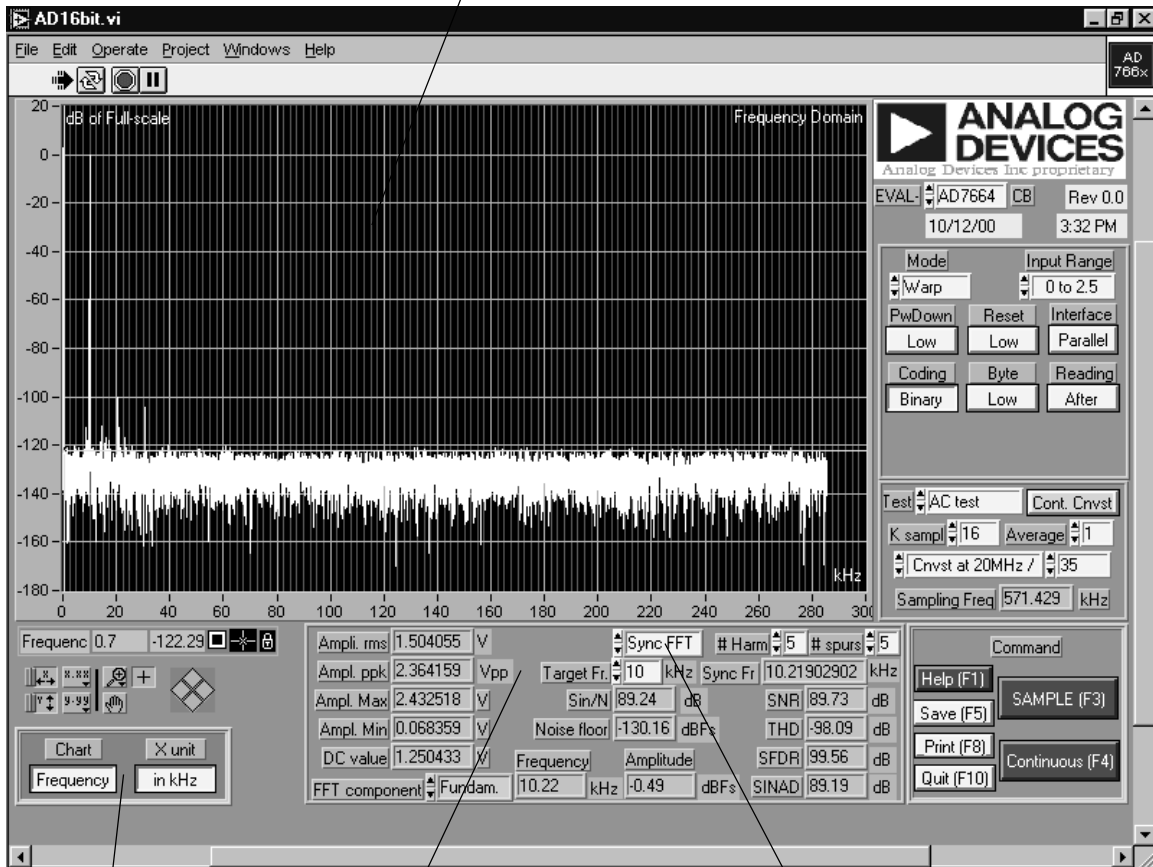


Figure 10. FFT Screen

This is the control that allows you the choice of either time domain or frequency domain. You may also change the X-axis unit here.

AC test results are shown here. You also have the choice of viewing the amplitude of a certain FFT component by changing the FFT component menu.

You may choose either a Kaiser window or a Blackmann-Harris window or a Sync FFT from this menu. . When choosing a Sync FFT, you will need to synchronize your analog source to the sampling frequency. The input frequency should be the value Sync Fr, which is to the right of Target frequency. The process for this is as follows:

1. You Choose a Target frequency
2. The software calculates an integer n based on the target frequency you entered and the sampling frequency, F_{samp}.
3. The software rounds up the value n to the next prime number.
4. The software then calculates the corresponding input frequency (F_{in}) and displays that as Sync Fr.

The equation, (capture window size) is shown below:
 $(1/F_{\text{samp}}) * (\text{number of samples}) = n * (1/F_{\text{in}})$

You can also view the output in the Time domain as shown below.

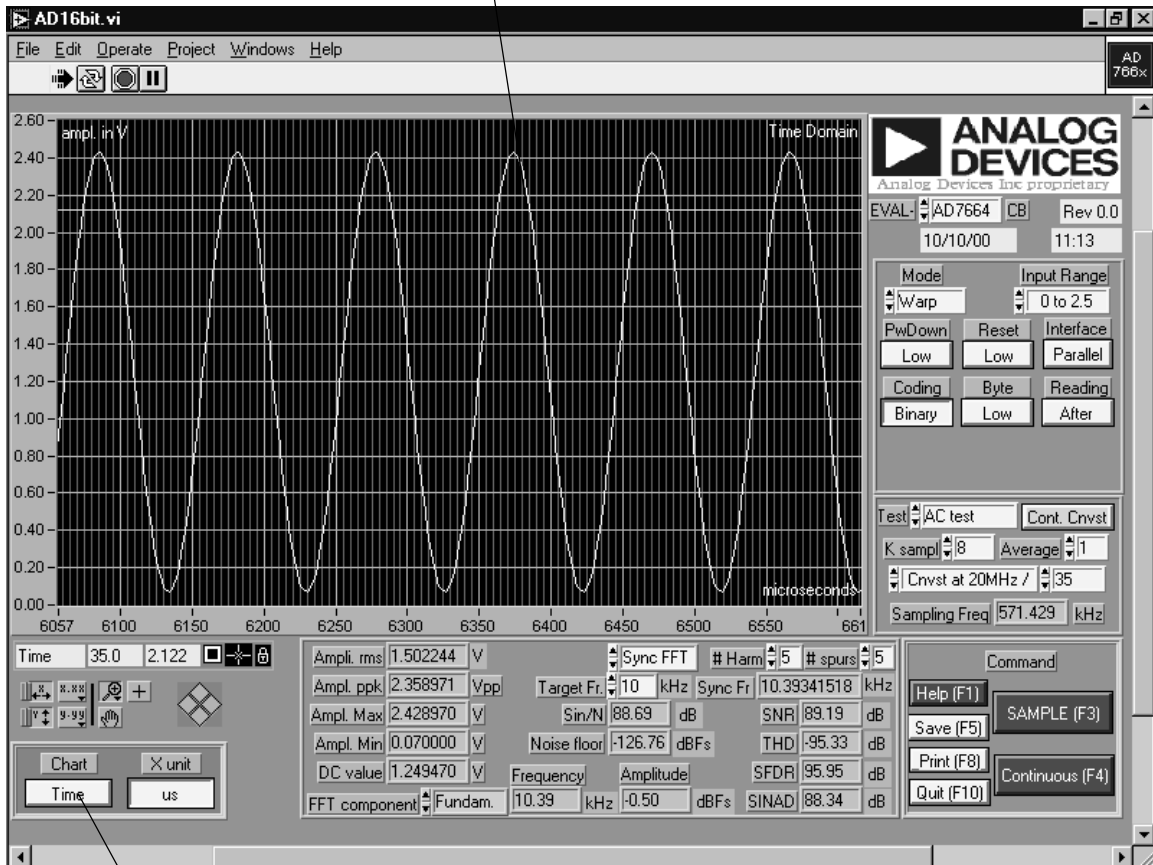


Figure 11. Time-Domain Screen

To view the Time domain, select Time in this menu.